



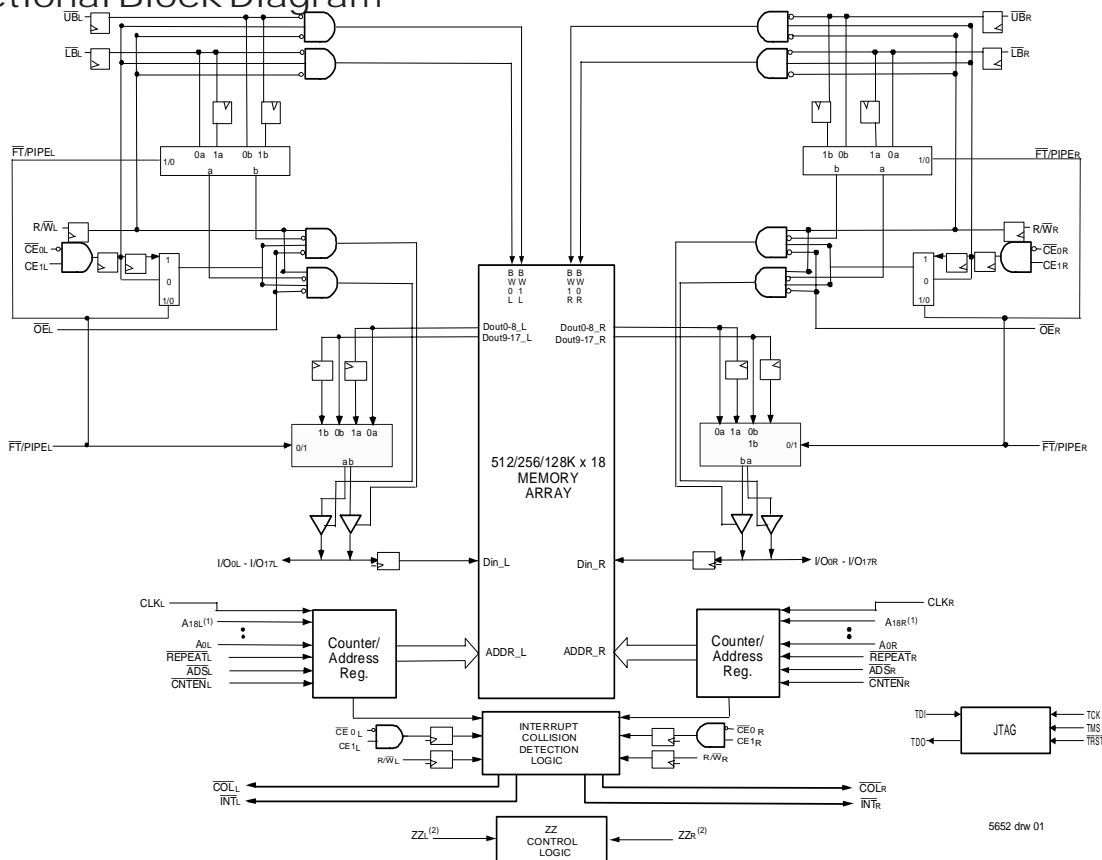
HIGH-SPEED 2.5V 512/256/128K X 18 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70T3339/19/99S

Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed data access
 - Commercial: 3.4 (200MHz)/3.6ns (166MHz)/4.2ns (133MHz)(max.)
 - Industrial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Interrupt and Collision Detection Flags
- ◆ Full synchronous operation on both ports
 - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
 - Fast 3.4ns clock to data out
 - 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
 - Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ Dual Cycle Deselect (DCD) for Pipelined Output Mode
- ◆ 2.5V ($\pm 100\text{mV}$) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V ($\pm 150\text{mV}$) or 2.5V ($\pm 100\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available at 166MHz and 133MHz
- ◆ Available in a 256-pin Ball Grid Array (BGA), a 144-pin Thin Quad Flatpack (TQFP) and 208-pin fine pitch Ball Grid Array (fpBGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1
- ◆ Due to limited pin count JTAG, Collision Detection and Interrupt are not supported on the 144-pin TQFP package
- ◆ Green parts available, see ordering information

Functional Block Diagram



NOTES:

1. Address A18 is a NC for the IDT70T3339. Also, Addresses A18 and A17 are NC's for the IDT70T3399.
2. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/FTx and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

JULY 2008

Description:

The IDT70T3339/19/99 is a high-speed 512/256/128k x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3339/19/99 has been optimized for applications having unidirec-

tional or bidirectional data flow in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70T3339/19/99 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) is at 2.5V.

Pin Configuration (3,4,5,6,9)

70T3339/19/99BC
BC-256⁽⁸⁾

256-Pin BGA
Top View⁽⁹⁾

01/13/03

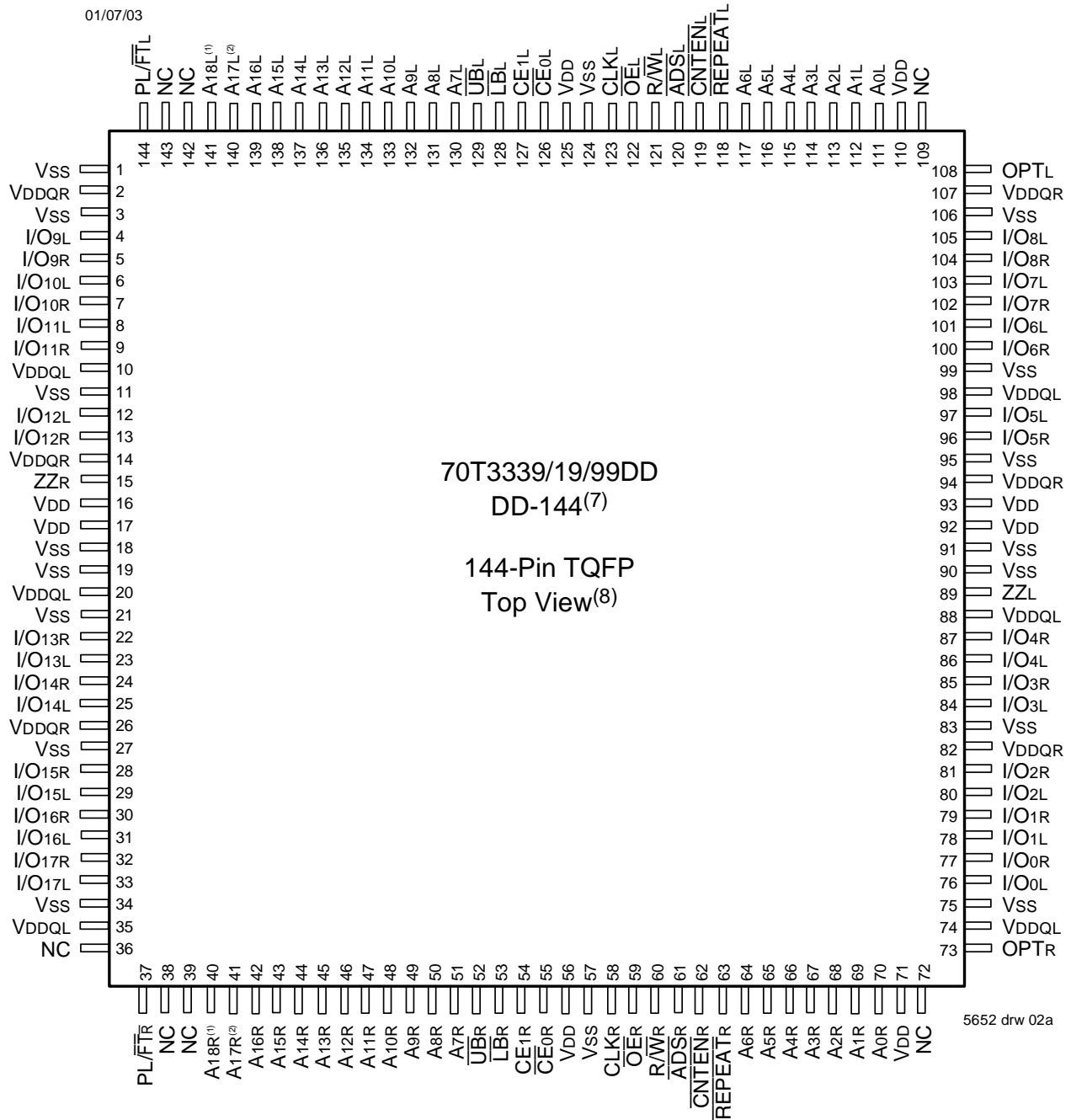
A1 NC	A2 TDI	A3 NC	A4 A17L ⁽²⁾	A5 A14L	A6 A11L	A7 A8L	A8 NC	A9 CE1L	A10 OE ⁻ L	A11 CNTENL	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 INT ⁻ L	B2 NC	B3 TDO	B4 A18L ⁽¹⁾	B5 A15L	B6 A12L	B7 A9L	B8 UB ⁻ L	B9 CE0L	B10 R/WL	B11 REPEATL	B12 A4L	B13 A1L	B14 VDD	B15 NC	B16 NC
C1 COLL	C2 I/O9L	C3 VSS	C4 A16L	C5 A13L	C6 A10L	C7 A7L	C8 NC	C9 LB ⁻ L	C10 CLKL	C11 ADSL	C12 A6L	C13 A3L	C14 OPTL	C15 NC	C16 I/O8L
D1 NC	D2 I/O9R	D3 NC	D4 PIPE/FTL	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 NC	D15 NC	D16 I/O8R
E1 I/O10R	E2 I/O10L	E3 NC	E4 VDDQL	E5 VDD	E6 VDD	E7 NC	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 NC	E15 I/O7L	E16 I/O7R
F1 I/O11L	F2 NC	F3 I/O11R	F4 VDDQL	F5 VDD	F6 NC	F7 NC	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O6R	F15 NC	F16 I/O6L
G1 NC	G2 NC	G3 I/O12L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O5L	G15 NC	G16 NC
H1 NC	H2 I/O12R	H3 NC	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 NC	H15 NC	H16 I/O5R
J1 I/O13L	J2 I/O14R	J3 I/O13R	J4 VDDQL	J5 ZZR	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 ZZL	J13 VDDQR	J14 I/O4R	J15 I/O3R	J16 I/O4L
K1 NC	K2 NC	K3 I/O14L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 NC	K15 NC	K16 I/O3L
L1 I/O15L	L2 NC	L3 I/O15R	L4 VDDQR	L5 VDD	L6 NC	L7 NC	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O2L	L15 NC	L16 I/O2R
M1 I/O16R	M2 I/O16L	M3 NC	M4 VDDQR	M5 VDD	M6 VDD	M7 NC	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O1R	M15 I/O1L	M16 NC
N1 NC	N2 I/O17R	N3 NC	N4 PIPE/FT ⁻ R	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 NC	N15 I/O0R	N16 NC
P1 COLR	P2 I/O17L	P3 TMS	P4 A16R	P5 A13R	P6 A10R	P7 A7R	P8 NC	P9 LB ⁻ R	P10 CLKR	P11 ADSR	P12 A6R	P13 A3R	P14 NC	P15 NC	P16 I/O0L
R1 INT ⁻ R	R2 NC	R3 TRST	R4 A18R ⁽¹⁾	R5 A15R	R6 A12R	R7 A9R	R8 UB ⁻ R	R9 CE0R	R10 R/W ⁻ R	R11 REPEATR	R12 A4R	R13 A1R	R14 OPTR	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A17R ⁽²⁾	T5 A14R	T6 A11R	T7 A8R	T8 NC	T9 CE1R	T10 OE ⁻ R	T11 CNTENR	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

5652 drw 02d

NOTES:

1. Pin is a NC for IDT70T3319 and IDT70T3399.
2. Pin is a NC for IDT70T3399.
3. All VDD pins must be connected to 2.5V power supply.
4. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VDD (2.5V), and 2.5V if OPT pin for that port is set to VSS (0V).
5. All VSS pins must be connected to ground supply.
6. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.
9. Pins A15 and T15 will be VREFL and VREFR respectively for future HSTL device.

Pin Configuration(con't)^(3,4,5,6,9,10)



NOTES:

1. Pin is a NC for IDT70T3319 and IDT70T3399.
2. Pin is a NC for IDT70T3399.
3. All V_{DD} pins must be connected to 2.5V power supply.
4. All V_{DD0} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{DD} (2.5V), and 2.5V if OPT pin for that port is set to V_{SS} (0V).
5. All V_{SS} pins must be connected to ground supply.
6. Package body is approximately 20mm x 20mm x 1.4mm.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.
9. Due to limited pin count, JTAG, Collision Detection and Interrupt are not supported in the DD-144 package.
10. Pins 109 and 72 will be V_{REFL} and V_{REFR} respectively for future HSTL device.

Pin Configurations(con't)^(3,4,5,6,9)

01/13/03

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
I/O _{9L}	$\overline{\text{INT}}_L$	V _{SS}	TDO	NC	A _{16L}	A _{12L}	A _{8L}	NC	V _{DD}	CLK _L	$\overline{\text{CNTEN}}_L$	A _{4L}	A _{0L}	OPT _L	NC	V _{SS}	A
NC	V _{SS}	$\overline{\text{COLL}}$	TDI	A _{17L} ⁽²⁾	A _{13L}	A _{9L}	NC	$\overline{\text{CE}}_{0L}$	V _{SS}	$\overline{\text{ADS}}_L$	A _{5L}	A _{1L}	NC	V _{DDQR}	I/O _{8L}	NC	B
V _{DDQL}	I/O _{9R}	V _{DDQR}	PIPE/ $\overline{\text{FT}}_L$	A _{18L} ⁽¹⁾	A _{14L}	A _{10L}	$\overline{\text{UB}}_L$	CE _{1L}	V _{SS}	R/ $\overline{\text{WL}}$	A _{6L}	A _{2L}	V _{DD}	I/O _{8R}	NC	V _{SS}	C
NC	V _{SS}	I/O _{10L}	NC	A _{15L}	A _{11L}	A _{7L}	$\overline{\text{LB}}_L$	V _{DD}	$\overline{\text{OE}}_L$	REPEAT _L	A _{3L}	V _{DD}	NC	V _{DDQL}	I/O _{7L}	I/O _{7R}	D
I/O _{11L}	NC	V _{DDQR}	I/O _{10R}	<p style="text-align: center;">70T3339/19/99BF BF-208⁽⁷⁾ 208-Pin fpBGA Top View⁽⁸⁾</p>									I/O _{6L}	NC	V _{SS}	NC	E
V _{DDQL}	I/O _{11R}	NC	V _{SS}										V _{SS}	I/O _{6R}	NC	V _{DDQR}	F
NC	V _{SS}	I/O _{12L}	NC										NC	V _{DDQL}	I/O _{5L}	NC	G
V _{DD}	NC	V _{DDQR}	I/O _{12R}										V _{DD}	NC	V _{SS}	I/O _{5R}	H
V _{DDQL}	V _{DD}	V _{SS}	ZZ _R										ZZ _L	V _{DD}	V _{SS}	V _{DDQR}	J
I/O _{14R}	V _{SS}	I/O _{13R}	V _{SS}										I/O _{3R}	V _{DDQL}	I/O _{4R}	V _{SS}	K
NC	I/O _{14L}	V _{DDQR}	I/O _{13L}										NC	I/O _{3L}	V _{SS}	I/O _{4L}	L
V _{DDQL}	NC	I/O _{15R}	V _{SS}										V _{SS}	NC	I/O _{2R}	V _{DDQR}	M
NC	V _{SS}	NC	I/O _{15L}										I/O _{1R}	V _{DDQL}	NC	I/O _{2L}	N
I/O _{16R}	I/O _{16L}	V _{DDQR}	$\overline{\text{COL}}_R$										TRST	A _{16R}	A _{12R}	A _{8R}	NC
V _{SS}	NC	I/O _{17R}	TCK	A _{17R} ⁽²⁾	A _{13R}	A _{9R}	NC	$\overline{\text{CE}}_{0R}$	V _{SS}	$\overline{\text{ADS}}_R$	A _{5R}	A _{1R}	NC	V _{DDQL}	I/O _{0R}	V _{DDQR}	R
NC	I/O _{17L}	V _{DDQL}	TMS	A _{18R} ⁽¹⁾	A _{14R}	A _{10R}	$\overline{\text{UB}}_R$	CE _{1R}	V _{SS}	R/ $\overline{\text{WR}}$	A _{6R}	A _{2R}	V _{SS}	NC	V _{SS}	NC	T
V _{SS}	$\overline{\text{INTR}}$	PIPE/ $\overline{\text{FT}}_R$	NC	A _{15R}	A _{11R}	A _{7R}	$\overline{\text{LB}}_R$	V _{DD}	$\overline{\text{OE}}_R$	REPEAT _R	A _{3R}	A _{0R}	V _{DD}	OPT _R	NC	I/O _{0L}	U

5652 drw 02c

NOTES:

1. Pin is a NC for IDT70T3319 and IDT70T3399.
2. Pin is a NC for IDT70T3399.
3. All V_{DD} pins must be connected to 2.5V power supply.
4. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{DD} (2.5V), and 2.5V if OPT pin for that port is set to V_{SS} (0V).
5. All V_{SS} pins must be connected to ground supply.
6. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.
9. Pins B14 and R14 will be V_{REFL} and V_{REFR} respectively for future HSTL device.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables (Input) ⁽⁷⁾
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable (Input)
\overline{OE}_L	\overline{OE}_R	Output Enable (Input)
A_{0L} - A_{18L} ⁽⁶⁾	A_{0R} - A_{18R} ⁽⁶⁾	Address (Input)
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
PL/\overline{FT}_L	PL/\overline{FT}_R	Pipeline/Flow-Through (Input)
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable (Input)
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable (Input)
\overline{REPEAT}_L	\overline{REPEAT}_R	Counter Repeat ⁽⁹⁾
\overline{UB}_L	\overline{UB}_R	Upper Byte Enable (I/O_9 - I/O_{17}) ⁽⁷⁾
\overline{LB}_L	\overline{LB}_R	Lower Byte Enable (I/O_0 - I/O_8) ⁽⁷⁾
V_{DD0L}	V_{DD0R}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾ (Input)
OPT_L	OPT_R	Option for selecting V_{DD0x} ^(1,2) (Input)
ZZ_L	ZZ_R	Sleep Mode pin ⁽⁴⁾ (Input)
V_{DD}		Power (2.5V) ⁽¹⁾ (Input)
V_{SS}		Ground (0V) (Input)
$TDI^{(5)}$		Test Data Input
$TDO^{(5)}$		Test Data Output
$TCK^{(5)}$		Test Logic Clock (10MHz) (Input)
$TMS^{(5)}$		Test Mode Select (Input)
$\overline{TRST}^{(5)}$		Reset (Initialize TAP Controller) (Input)
$\overline{INT}_L^{(5)}$	$\overline{INT}_R^{(5)}$	Interrupt Flag (Output)
$\overline{COL}_L^{(5)}$	$\overline{COL}_R^{(5)}$	Collision Alert (Output)

5652 tbl 01

NOTES:

- V_{DD} , $OPTx$, and V_{DD0x} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- $OPTx$ selects the operating voltage levels for the I/Os and controls on that port. If $OPTx$ is set to V_{DD} (2.5V), then that port's I/Os and controls will operate at 3.3V levels and V_{DD0x} must be supplied at 3.3V. If $OPTx$ is set to V_{SS} (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DD0x} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
- When \overline{REPEAT}_x is asserted, the counter will reset to the last valid address loaded via \overline{ADS}_x .
- The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/\overline{FT}_x and $OPTx$ and the sleep mode pins themselves (ZZx) are not affected during sleep mode. It is recommended that boundary scan not be operated during sleep mode.
- Due to limited pin count, JTAG, Collision Detection and Interrupt are not supported in the DD-144 package.
- Address A_{18x} is a NC for the IDT70T3319. Also, Addresses A_{18x} and A_{17x} are NC's for the IDT70T3399.
- Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control (1,2,3,4)

\overline{OE}	CLK	\overline{CE}_0	CE ₁	\overline{UB}	\overline{LB}	R \overline{W}	ZZ	Upper Byte I/O ₉₋₁₇	Lower Byte I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	L	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	L	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	L	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	H	L	L	L	High-Z	D _{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	L	D _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	L	D _{IN}	D _{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	L	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	L	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	L	D _{OUT}	D _{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	L	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	H	High-Z	High-Z	Sleep Mode

5652 tbl 02

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{REPEAT} = X.
- \overline{OE} and ZZ are asynchronous input signals.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control (1,2)

Address	Previous Internal Address	Internal Address Used	CLK	\overline{ADS}	\overline{CNTEN}	$\overline{REPEAT}^{(6)}$	I/O ⁽³⁾	MODE
An	X	An	↑	L ⁽⁴⁾	X	H	D _{I/O} (n)	External Address Used
X	An	An + 1	↑	H	L ⁽⁵⁾	H	D _{I/O} (n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	D _{I/O} (n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L ⁽⁴⁾	D _{I/O} (n)	Counter Set to last valid \overline{ADS} load

5652 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R \overline{W} , \overline{CE}_0 , CE₁, \overline{UB} , \overline{LB} and \overline{OE} .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and \overline{REPEAT} are independent of all other memory control signals including \overline{CE}_0 , CE₁, \overline{UB} and \overline{LB} .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including \overline{CE}_0 , CE₁, \overline{UB} and \overline{LB} .
- When \overline{REPEAT} is asserted, the counter will reset to the last valid address loaded via \overline{ADS} . This value is not set at power-up: a known location should be loaded via \overline{ADS} during initialization if desired. Any subsequent \overline{ADS} access during operations will update the \overline{REPEAT} address location.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	2.5V ± 100mV
Industrial	-40°C to +85°C	0V	2.5V ± 100mV

5652 tbl 04

NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address, Control & Data I/O Inputs) ⁽³⁾	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG	1.7	—	V _{DD} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, OPT, PIPE/ \overline{FT}	V _{DD} - 0.2V	—	V _{DD} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V
V _{IL}	Input Low Voltage - ZZ, OPT, PIPE/ \overline{FT}	-0.3 ⁽¹⁾	—	0.2	V

5652 tbl 05a

NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{SS}(0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address, Control & Data I/O Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG	1.7	—	V _{DD} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, OPT, PIPE/ \overline{FT}	V _{DD} - 0.2V	—	V _{DD} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V
V _{IL}	Input Low Voltage - ZZ, OPT, PIPE/ \overline{FT}	-0.3 ⁽¹⁾	—	0.2	V

5652 tbl 05b

NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than tcyc/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{DD} (2.5V), and V_{DDQX} for that port must be supplied as indicated above.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} (V _{DD})	V _{DD} Terminal Voltage with Respect to GND	-0.5 to 3.6	V
V _{TERM} ⁽²⁾ (V _{DDQ})	V _{DDQ} Terminal Voltage with Respect to GND	-0.3 to V _{DDQ} + 0.3	V
V _{TERM} ⁽²⁾ (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	-0.3 to V _{DDQ} + 0.3	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT} (For V _{DDQ} = 3.3V)	DC Output Current	50	mA
I _{OUT} (For V _{DDQ} = 2.5V)	DC Output Current	40	mA

5652 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

Capacitance⁽¹⁾

(T_A = +25°C, f = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

5652 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T3339/19/99S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LI}	JTAG & ZZ Input Leakage Current ^(1,2)	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	±30	μA
I _{LO}	Output Leakage Current ^(1,3)	$\overline{CE}_0 = V_{IH}$ or CE ₁ = V _{IL} , V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽¹⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽¹⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽¹⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽¹⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

5652 tbl 08

NOTES:

- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.6 for details.
- Applicable only for TMS, TDI and TRST inputs.
- Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ⁽³⁾ ($V_{DD} = 2.5V \pm 100mV$)

Symbol	Parameter	Test Condition	Version	70T3339/19/99 S200 Com'l Only ⁽⁶⁾		70T3339/19/99 S166 Com'l & Ind ⁽⁷⁾		70T3339/19/99 S133 Com'l & Ind		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
I _{DD}	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	375	525	320	450	260	370	mA
			IND	S	—	—	320	510	260	450	
I _{SB1} ⁽⁶⁾	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	205	270	175	230	140	190	mA
			IND	S	—	—	175	275	140	235	
I _{SB2} ⁽⁶⁾	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	300	375	250	325	200	250	mA
			IND	S	—	—	250	365	200	310	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	5	15	5	15	5	15	mA
			IND	S	—	—	5	20	5	20	
I _{SB4} ⁽⁶⁾	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	300	375	250	325	200	250	mA
			IND	S	—	—	250	365	200	310	
I _{ZZ}	Sleep Mode Current (Both Ports - TTL Level Inputs)	$ZZ_L = ZZ_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	5	15	5	15	5	15	mA
			IND	S	—	—	5	20	5	20	

NOTES:

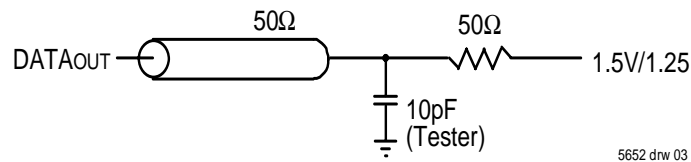
5652 Ibl 09

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS".
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 2.5V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} dc(f=0) = 15mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} = 0.2V$
"X" represents "L" for left port or "R" for right port.
- I_{SB1}, I_{SB2} and I_{SB4} will all reach full standby levels (I_{SB3}) on the appropriate port(s) if ZZ_L and/or ZZ_R = V_{IH}.
- 166MHz I-Temp is not available in the BF-208 package.
- 200Mhz is not available in the BF-208 and DD-144 packages.

AC Test Conditions ($V_{DDQ} = 3.3V/2.5V$)

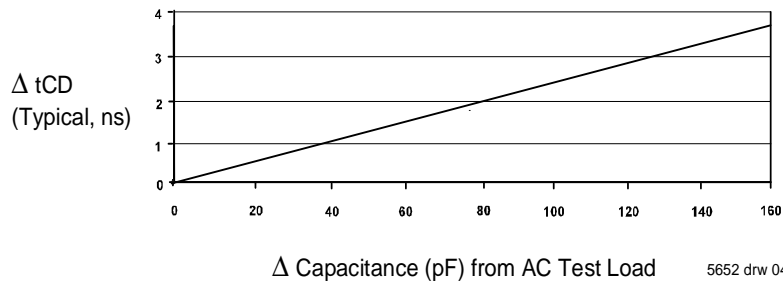
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5652 tbl 10



5652 drw 03

Figure 1. AC Output Test load.



5652 drw 04

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) ^(2,3) ($V_{DD} = 2.5V \pm 100mV$, $T_A = 0^\circ C$ to $+70^\circ C$)

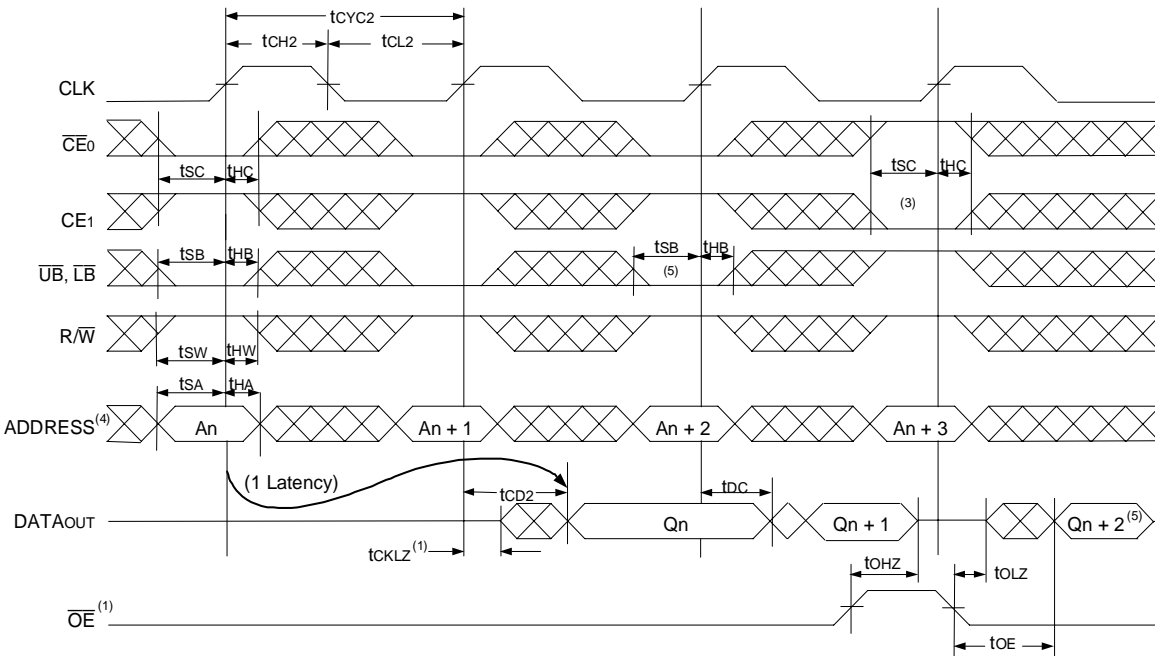
Symbol	Parameter	70T3339/19/99 S200 Com'l Only ⁽⁵⁾		70T3339/19/99 S166 Com'l & Ind ⁽⁴⁾		70T3339/19/99 S133 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽¹⁾	15	—	20	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽¹⁾	5	—	6	—	7.5	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽¹⁾	6	—	8	—	10	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽¹⁾	6	—	8	—	10	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	2	—	2.4	—	3	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽¹⁾	2	—	2.4	—	3	—	ns
t _{SA}	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SC}	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HC}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SB}	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HB}	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SW}	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HW}	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SD}	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HD}	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SRPT}	\overline{REPEAT} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HRPT}	\overline{REPEAT} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{OE}	Output Enable to Data Valid	—	4.4	—	4.4	—	4.6	ns
t _{OLZ} ⁽⁶⁾	Output Enable to Output Low-Z	1	—	1	—	1	—	ns
t _{OHZ} ⁽⁶⁾	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	10	—	12	—	15	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.4	—	3.6	—	4.2	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ} ⁽⁶⁾	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CKLZ} ⁽⁶⁾	Clock High to Output Low-Z	1	—	1	—	1	—	ns
t _{INS}	Interrupt Flag Set Time	—	7	—	7	—	7	ns
t _{INR}	Interrupt Flag Reset Time	—	7	—	7	—	7	ns
t _{COLS}	Collision Flag Set Time	—	3.4	—	3.6	—	4.2	ns
t _{COLR}	Collision Flag Reset Time	—	3.4	—	3.6	—	4.2	ns
t _{ZZSC}	Sleep Mode Set Cycles	2	—	2	—	2	—	cycles
t _{ZZRC}	Sleep Mode Recovery Cycles	3	—	3	—	3	—	cycles
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	4	—	5	—	6	—	ns
t _{OF}	Clock-to-Clock Offset for Collision Detection	Please refer to Collision Detection Timing Table on Page 21						

5652 tbl 11

NOTES:

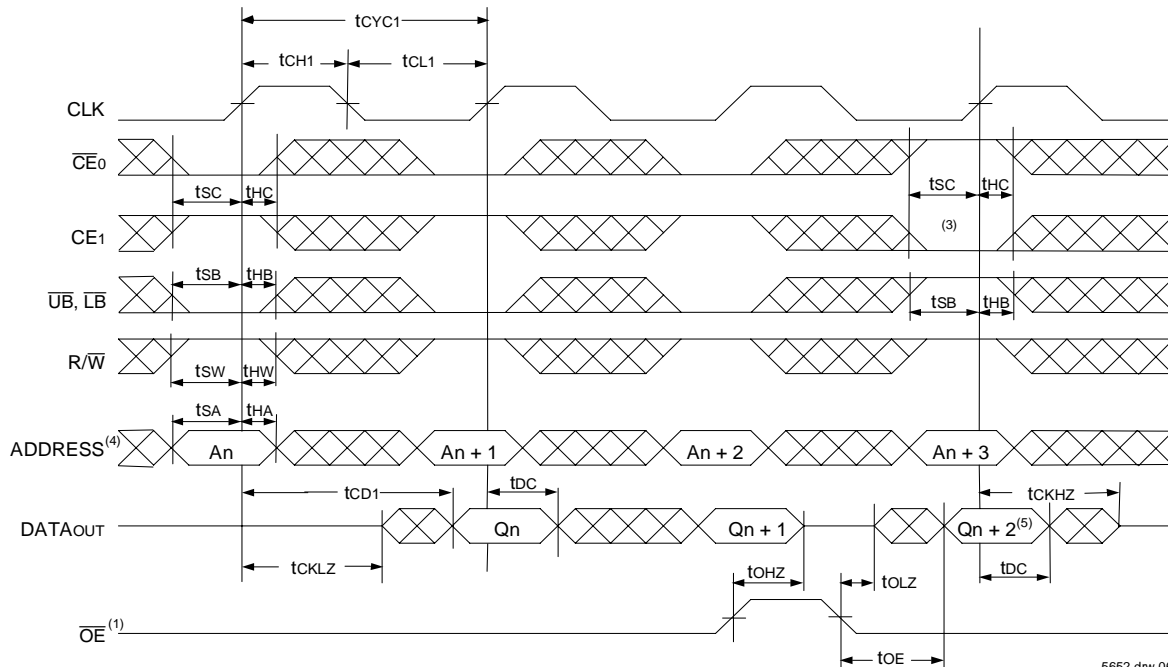
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPEx = V_{DD}$ (2.5V). Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{SS}$ (0V) for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}), $\overline{FT}/PIPE$ and OPT. $\overline{FT}/PIPE$ and OPT should be treated as DC signals, i.e. steady state during operation.
- These values are valid for either level of V_{DD0} (3.3V/2.5V). See page 6 for details on selecting the desired operating voltage levels for each port.
- 166MHz I-Temp is not available in the BF-208 package.
- 200MHz is not available in the BF-208 and DD-144 packages.
- Guaranteed by design (not production tested).

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}/PIPE'X' = V_{IH}$)⁽²⁾



5652 drw 05

Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}/PIPE'X' = V_{IL}$)^(2,6)

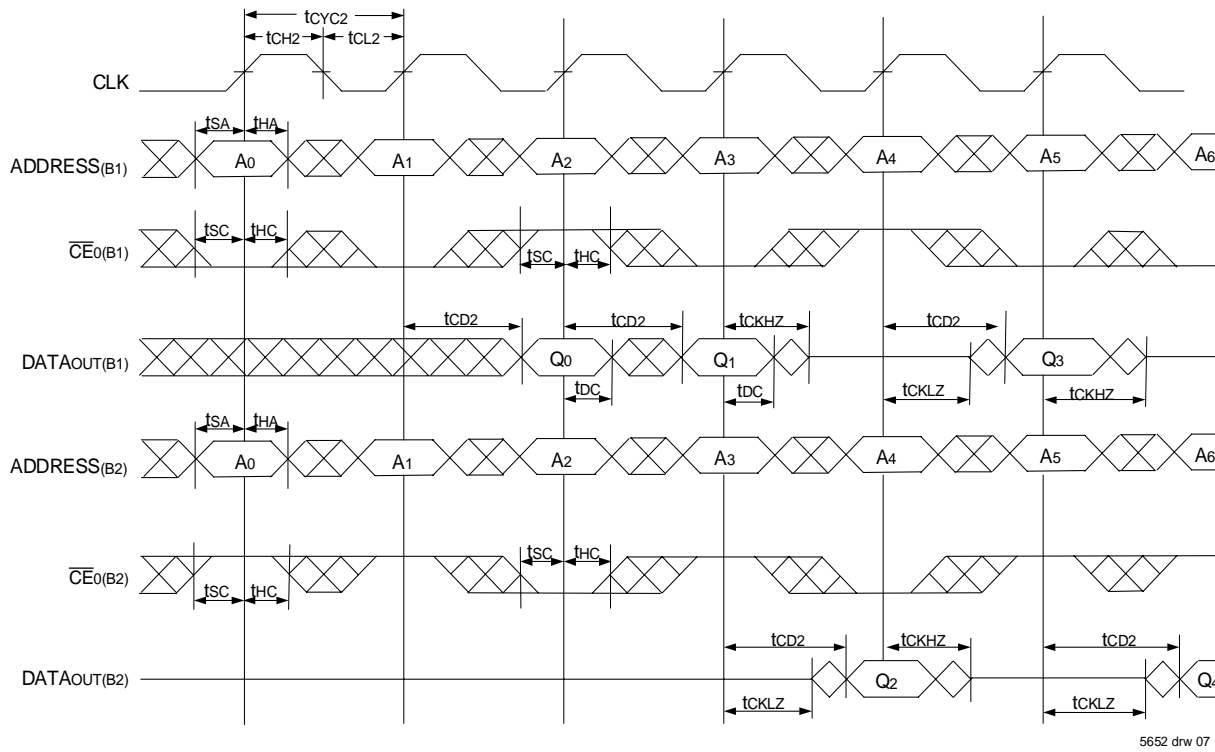


5652 drw 06

NOTES:

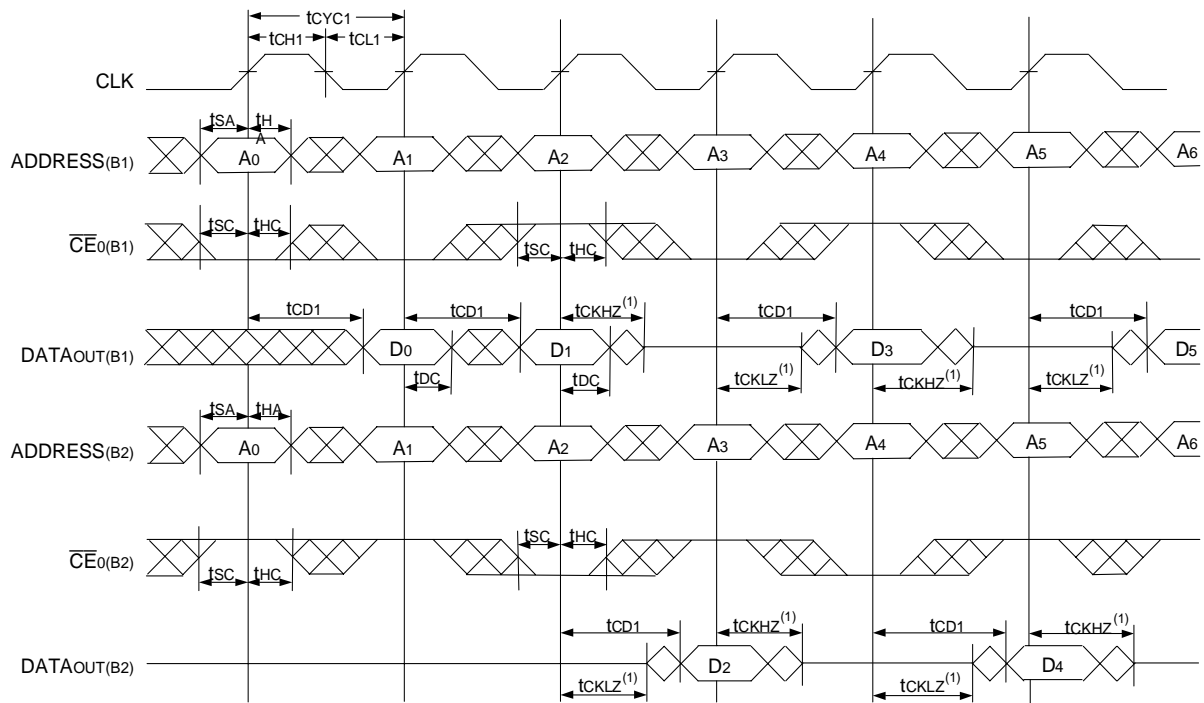
1. \overline{OE} is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{REPEAT} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE0} = V_{IH}$, $CE1 = V_{IL}$, \overline{UB} , $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{UB} , \overline{LB} was HIGH, then the appropriate Byte of DATAout for $Qn + 2$ would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read^(1,2)



5652 drw 07

Timing Waveform of a Multi-Device Flow-Through Read^(1,2)

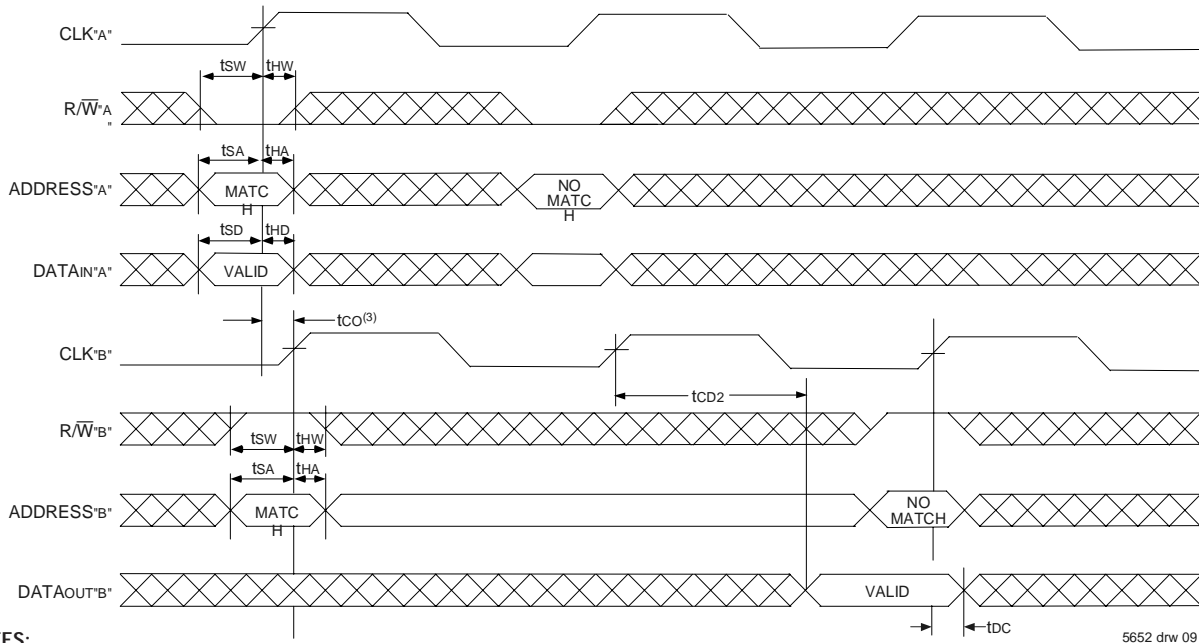


5652 drw 08

NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70T3339/19/99 for this waveform, and are setup for depth expansion in this example. ADDRESS_(B1) = ADDRESS_(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and \overline{ADS} = VIH; $\overline{CE1}$ (B1), $\overline{CE1}$ (B2), \overline{RW} , \overline{CNTEN} , and \overline{REPEAT} = VIH.

Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2,4)

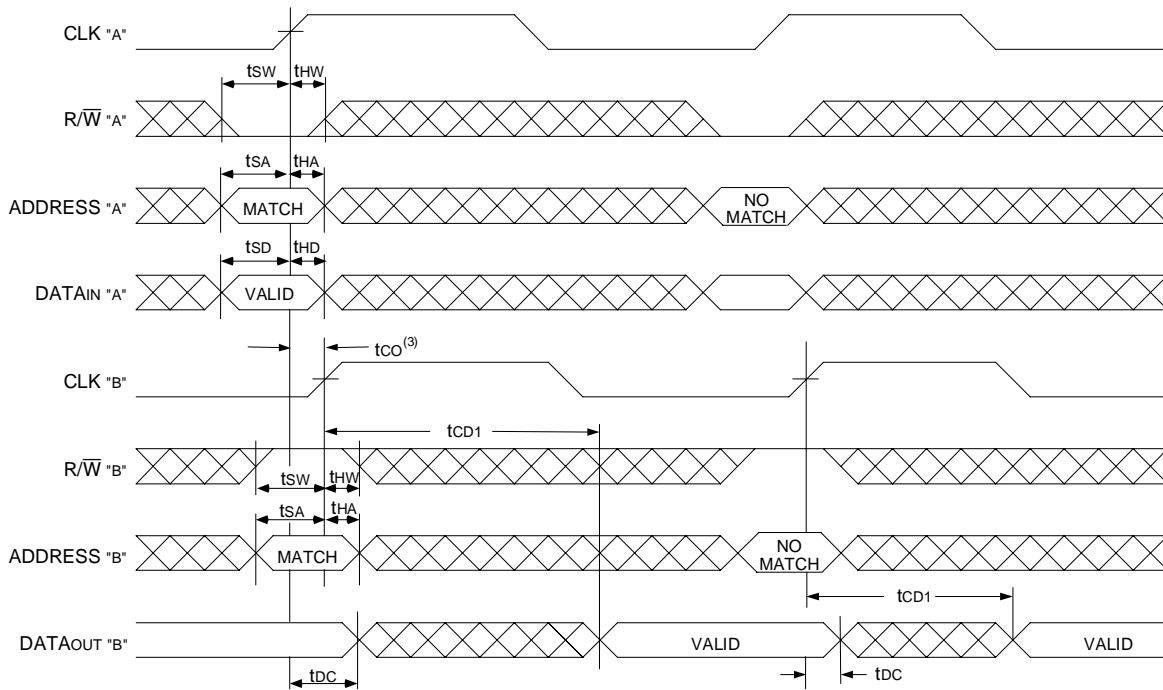


NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for Port "B", which is being read from. $\overline{OE} = V_{IH}$ for Port "A", which is being written to.
3. If $t_{co} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + 2 t_{cyc} + t_{cd2}$). If $t_{co} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + t_{cyc} + t_{cd2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right ports. Port "B" is the opposite of Port "A"

5652 drw 09

Timing Waveform with Port-to-Port Flow-Through Read^(1,2,4)



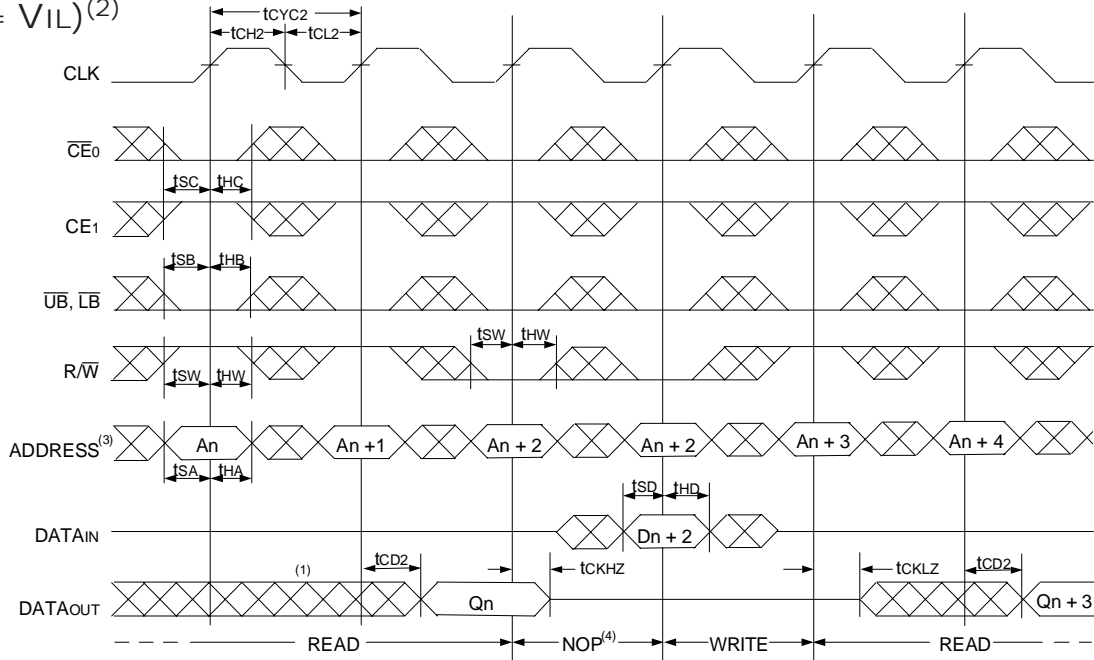
NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{co} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{co} + t_{cyc} + t_{cd1}$). If $t_{co} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{co} + t_{cd1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

5652 drw 10

Timing Waveform of Pipelined Read-to-Write-to-Read

($\overline{OE} = V_{IL}$)⁽²⁾

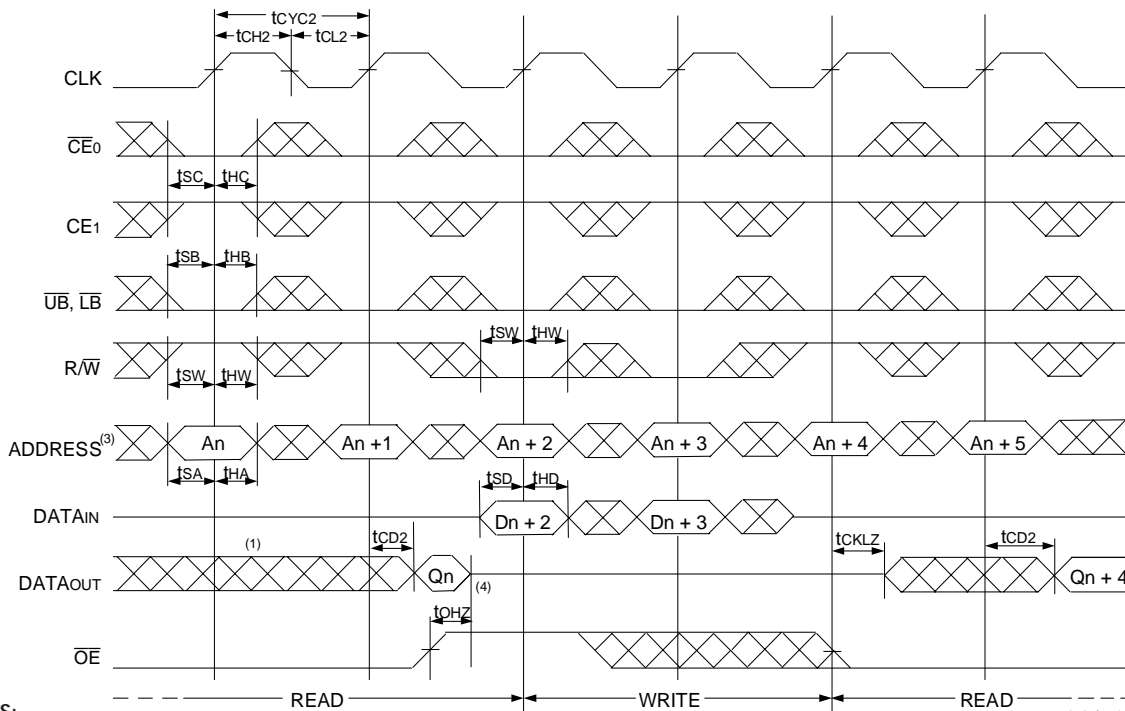


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

5652 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

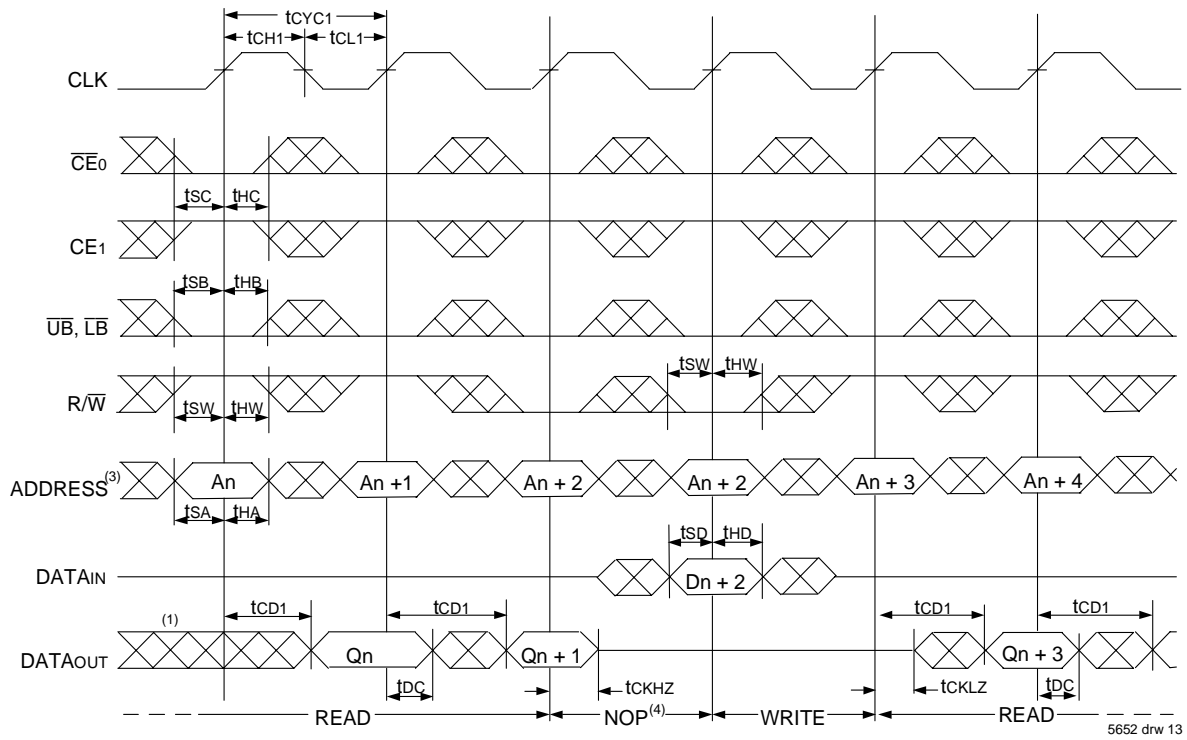


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

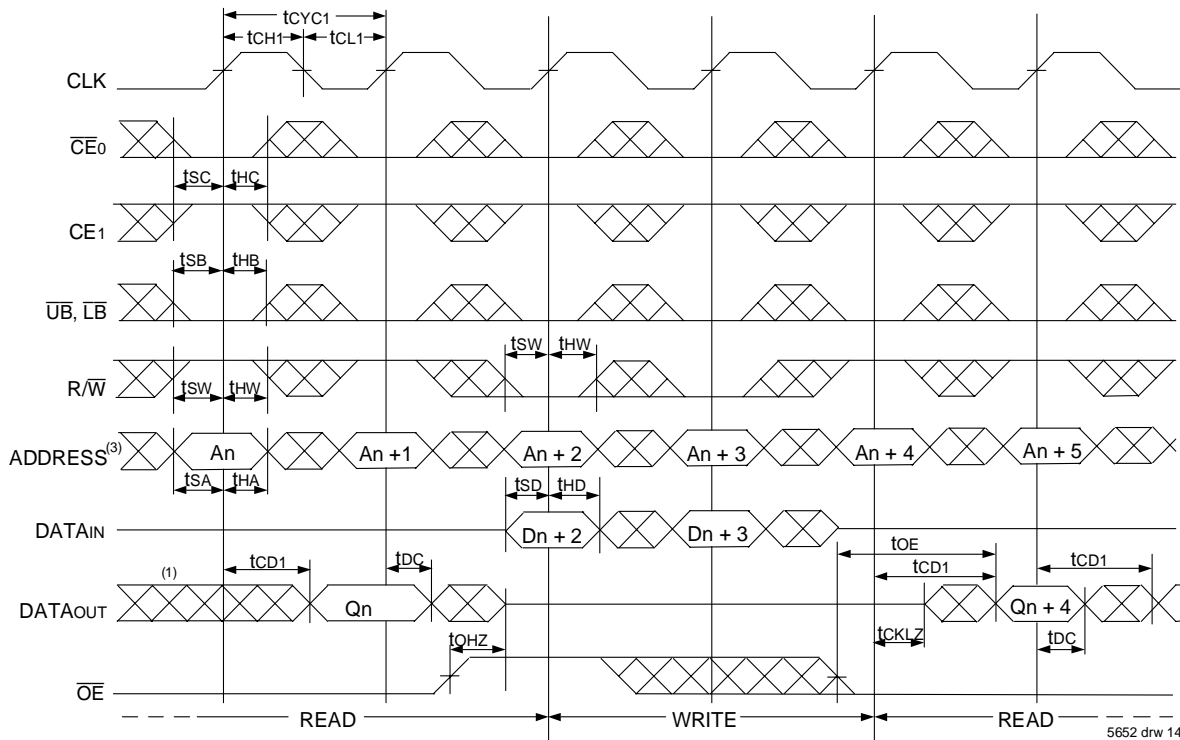
5652 drw 12

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



5652 drw 13

Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

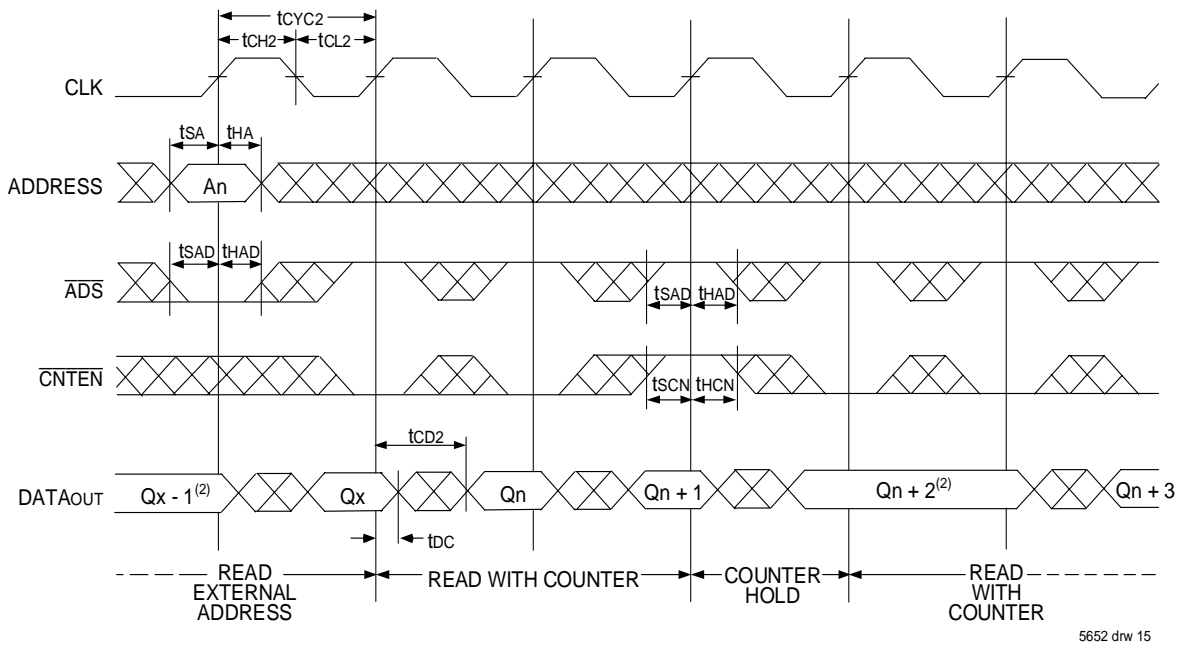


5652 drw 14

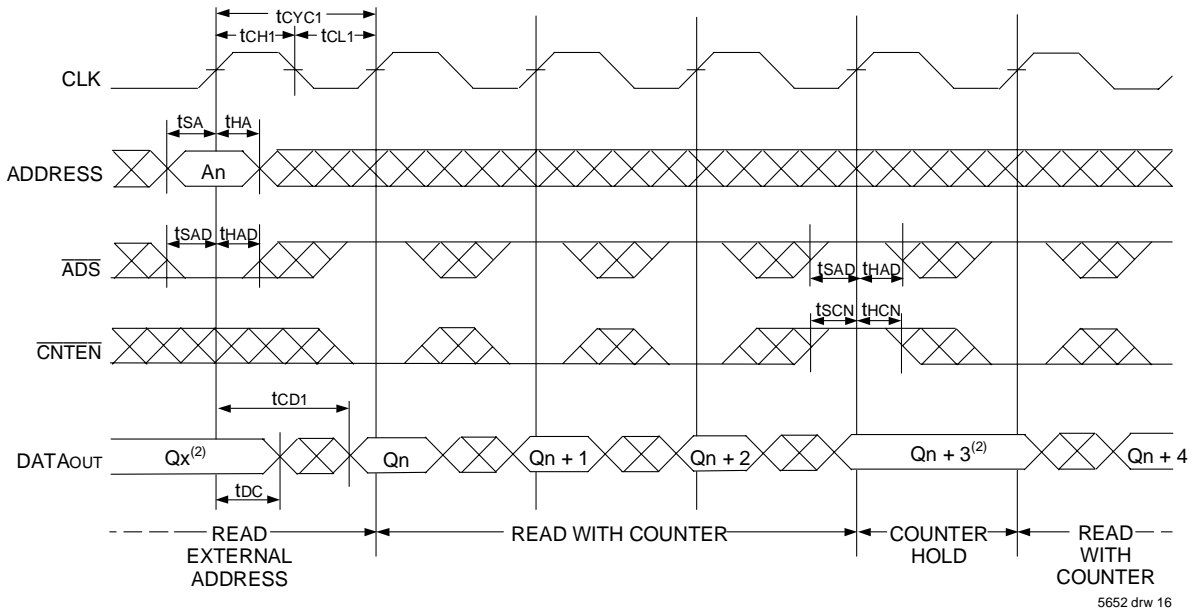
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



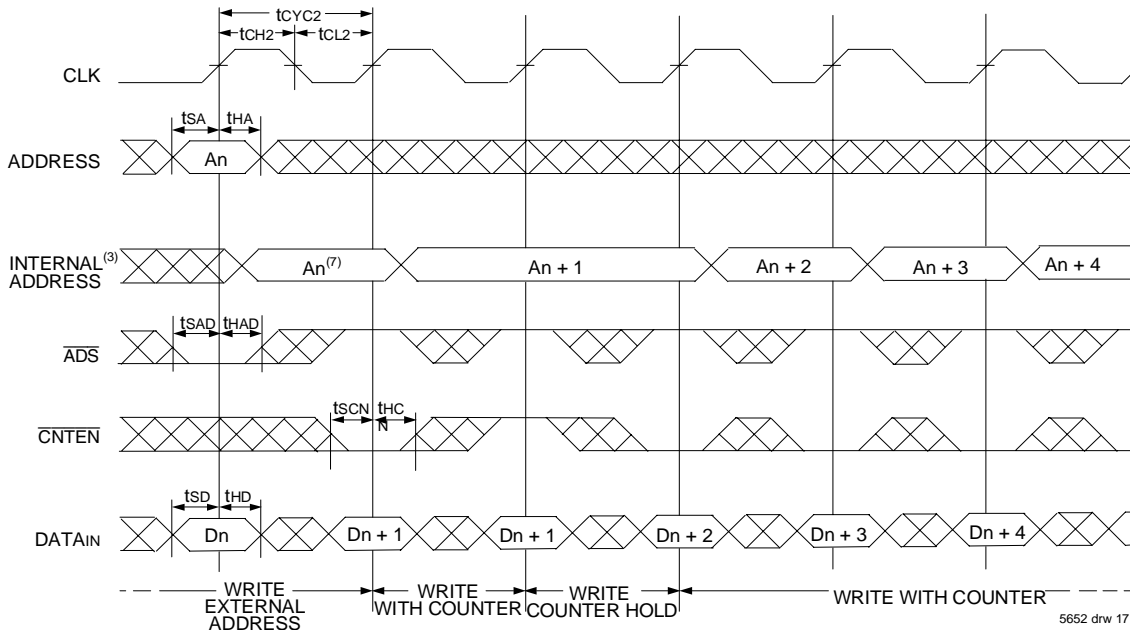
Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾



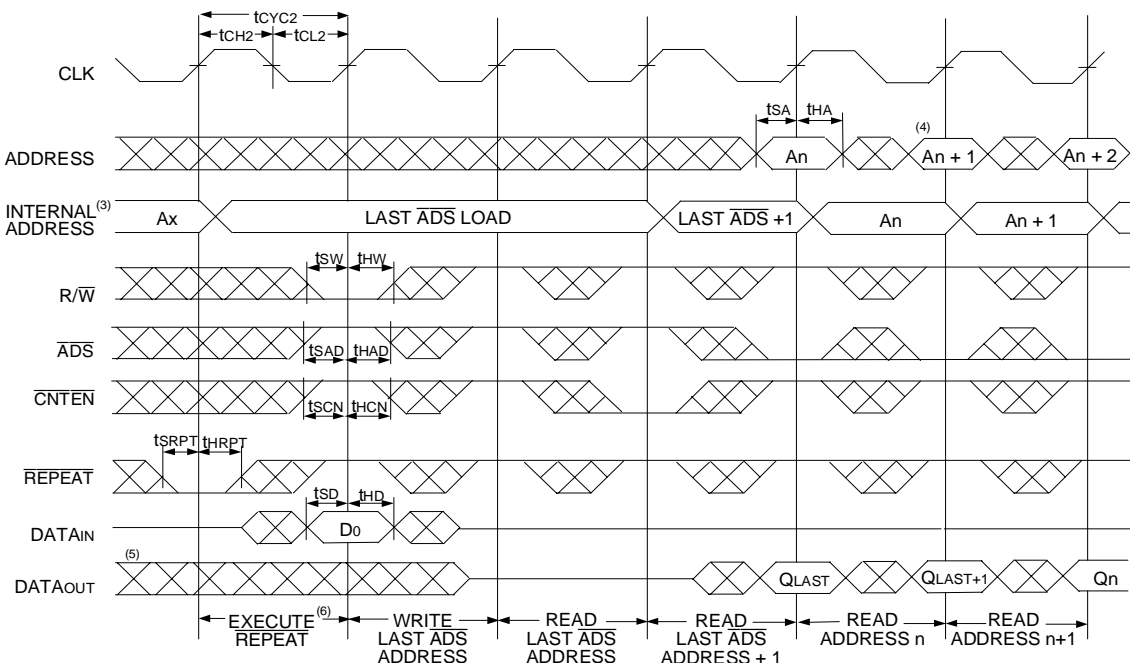
NOTES:

1. $\overline{CE_0}$, \overline{OE} , \overline{UB} , $\overline{LB} = V_{IL}$; $\overline{CE_1}$, $\overline{R/W}$, and $\overline{REPEAT} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)⁽¹⁾



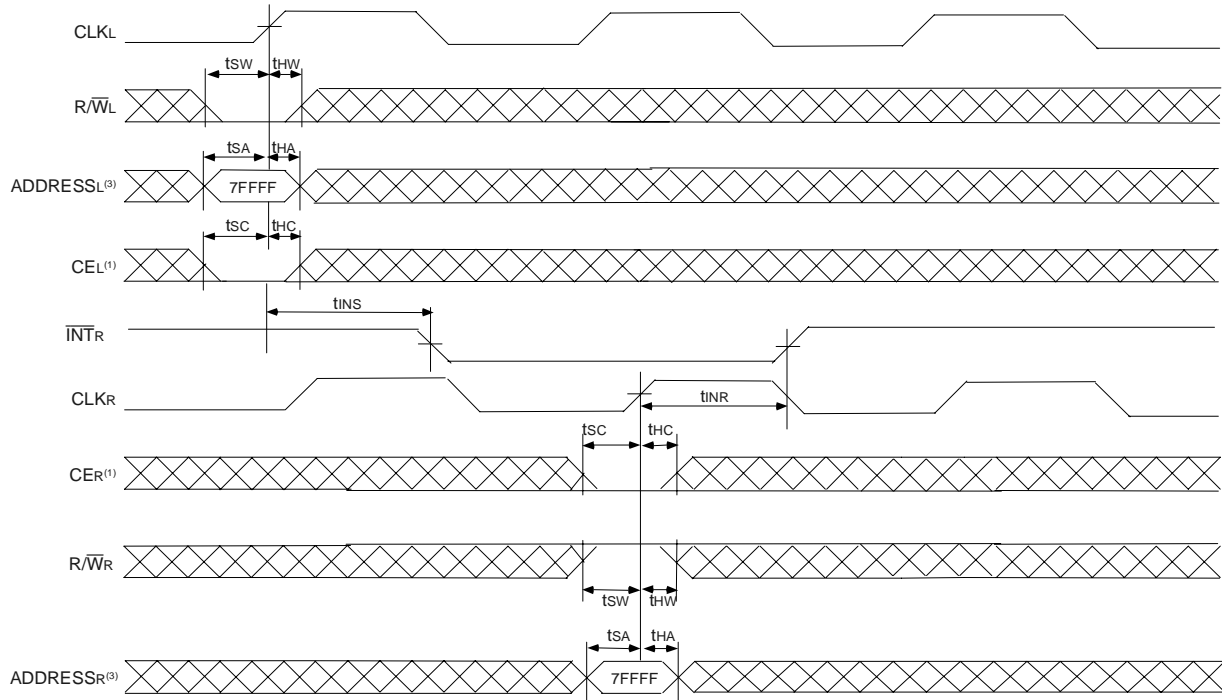
Timing Waveform of Counter Repeat⁽²⁾



NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and R/\overline{W} = V_{IL} ; CE_1 and \overline{REPEAT} = V_{IH} .
2. \overline{CE}_0 , \overline{UB} , \overline{LB} = V_{IL} ; CE_1 = V_{IH} .
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during \overline{REPEAT} operation. A READ or WRITE cycle may be coincidental with the counter \overline{REPEAT} cycle: Address loaded by last valid \overline{ADS} load will be accessed. Extra cycles are shown here simply for clarification. For more information on \overline{REPEAT} function refer to Truth Table II.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Waveform of Interrupt Timing (2)



5652 drw 19

NOTES:

1. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Truth Table III – Interrupt Flag (1)

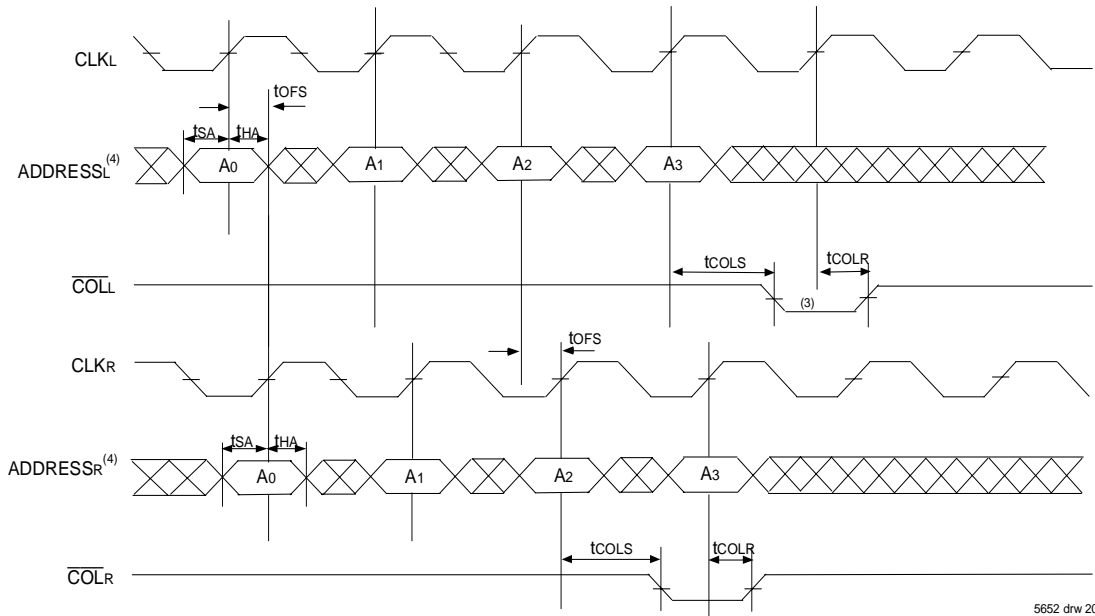
Left Port					Right Port					Function
CLKL	R/WL ⁽²⁾	CEL ⁽²⁾	A18L-A0L ^(3,4,5)	INTL	CLKR	R/WR ⁽²⁾	CER ⁽²⁾	A18R-A0R ^(3,4,5)	INTR	
↑	L	L	7FFFF	X	↑	X	X	X	L	Set Right \overline{INTR} Flag
↑	X	X	X	X	↑	H	L	7FFFF	H	Reset Right \overline{INTR} Flag
↑	X	X	X	L	↑	L	L	7FFFE	X	Set Left \overline{INTL} Flag
↑	H	L	7FFFE	H	↑	X	X	X	X	Reset Left \overline{INTL} Flag

5652 tbl 12

NOTES:

1. \overline{INTL} and \overline{INTR} must be initialized at power-up by Resetting the flags.
2. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. R/W and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. A18x is a NC for IDT70T3319, therefore Interrupt Addresses are 3FFFF and 3FFFE.
4. A18x and A17x are NC's for IDT70T3399, therefore Interrupt Addresses are 1FFFF and 1FFFE.
5. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Waveform of Collision Timing (1,2) Both Ports Writing with Left Port Clock Leading



NOTES:

1. $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$.
2. For reading port, \overline{OE} is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output $3t_{CYC2} + t_{COLS}$ after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Collision Detection Timing (3,4)

Cycle Time	t _{ofs} (ns)	
	Region 1 (ns) ⁽¹⁾	Region 2 (ns) ⁽²⁾
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

5652 tbl 13

NOTES:

1. **Region 1**
Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. **Region 2**
Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

Truth Table IV — Collision Detection Flag

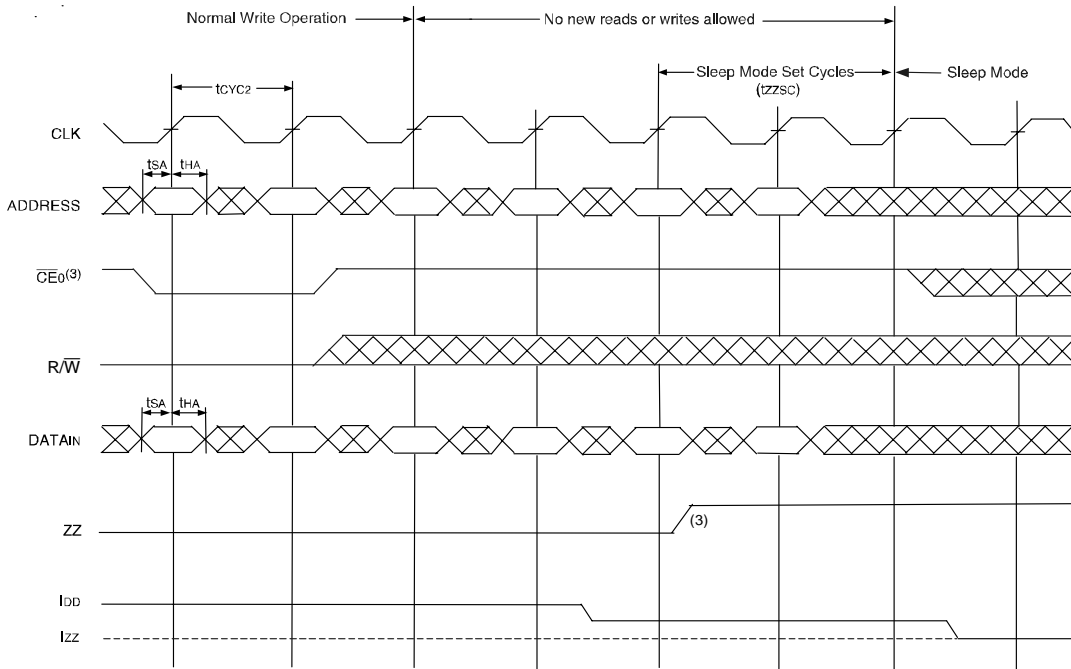
Left Port					Right Port					Function
CLKL	R/W _L ⁽¹⁾	CE _L ⁽¹⁾	A _{18L} -A _{0L} ⁽²⁾	\overline{COLL}	CLKR	R/W _R ⁽¹⁾	CE _R ⁽¹⁾	A _{18R} -A _{0R} ⁽²⁾	\overline{COLR}	
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port.
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

NOTES:

1. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. R/W and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

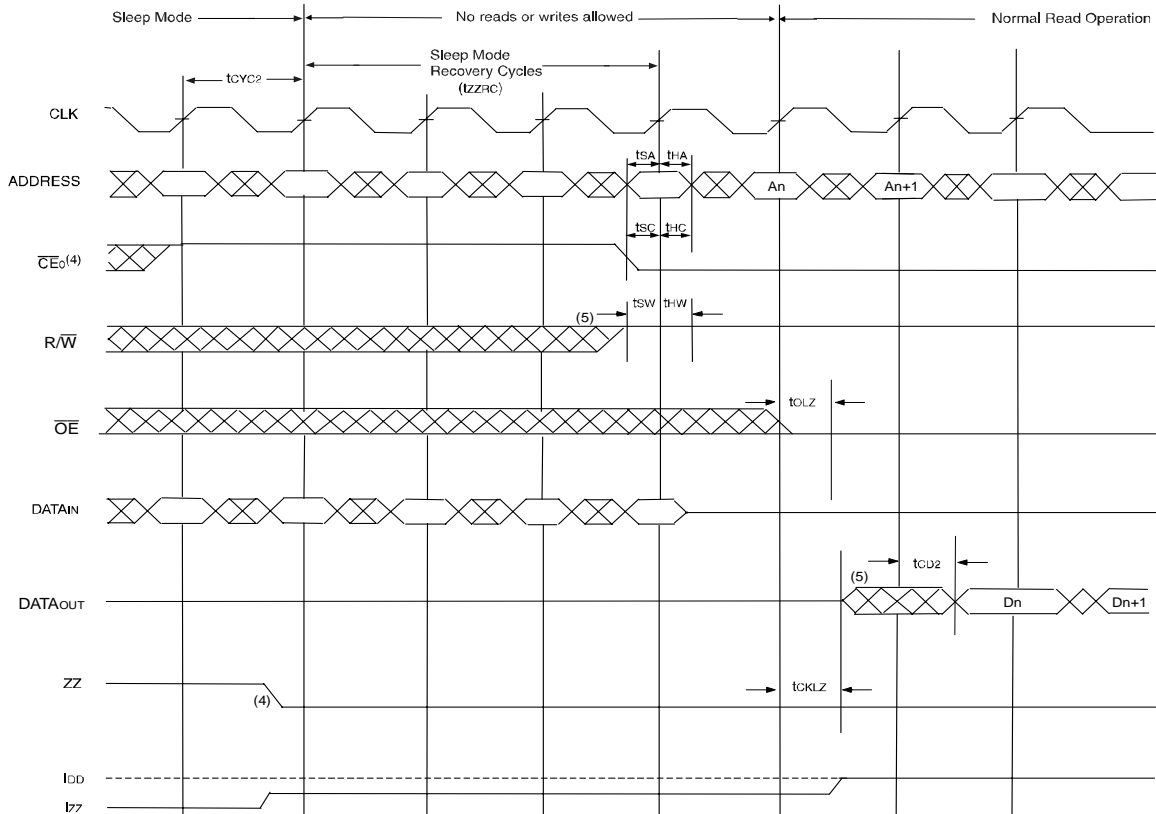
5652 tbl 14

Timing Waveform - Entering Sleep Mode (1,2)



5652 drw 22

Timing Waveform - Exiting Sleep Mode (1,2)



5652 drw 22a

NOTES:

1. CE1 = VIH.
2. All timing is same for Left and Right ports.
3. CE0 has to be deactivated (CE0 = VIH) three cycles prior to asserting ZZ (ZZx = VIH) and held for two cycles after asserting ZZ (ZZx = VIH).
4. CE0 has to be deactivated (CE0 = VIH) one cycle prior to de-asserting ZZ (ZZx = VIL) and held for three cycles after de-asserting ZZ (ZZx = VIL).
5. The device must be in Read Mode (R/W High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

Functional Description

The IDT70T3339/19/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE0}$ or a LOW on CE1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3339/19/99s for depth expansion configurations. Two cycles are required with $\overline{CE0}$ LOW and CE1 HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INTL}) is asserted when the right port writes to memory location 7FFFE (HEX), where a write is defined as $\overline{CE_R} = R/\overline{W_R} = V_{IL}$ per the Truth Table. The left port clears the interrupt through access of address location 7FFFE when $\overline{CE_L} = V_{IL}$ and $R/\overline{W_L} = V_{IH}$. Likewise, the right port interrupt flag (\overline{INTR}) is asserted when the left port writes to memory location 7FFFF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must read the memory location 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399). The message (18 bits) at 7FFFE or 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFFE and 7FFFF (3FFFF or 3FFFE for IDT70T3319 and 1FFFF or 1FFFE for IDT70T3399) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detection

Collision is defined as an overlap in access between the two ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($\overline{COL_x}$) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on Page 21. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert

flag. A third collision will generate the alert flag as appropriate. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on page 21.

Collision detection on the IDT70T3339/19/99 represents a significant advance in functionality over current sync multi-ports, which have no such capability. In addition to this functionality the IDT70T3339/19/99 sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70T3339/19/99 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

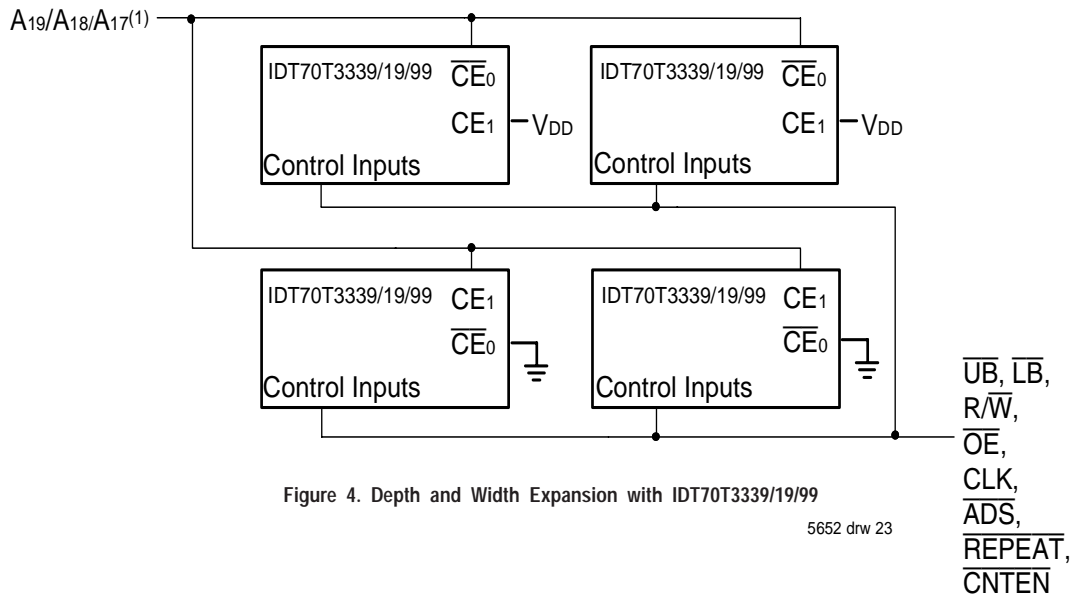
For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ ($ZZ_x = V_{IH}$) and three cycles after de-asserting ZZ ($ZZ_x = V_{IL}$), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode ($R/\overline{W}_x = V_{IH}$) when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAM's sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Depth and Width Expansion

The IDT70T3339/19/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

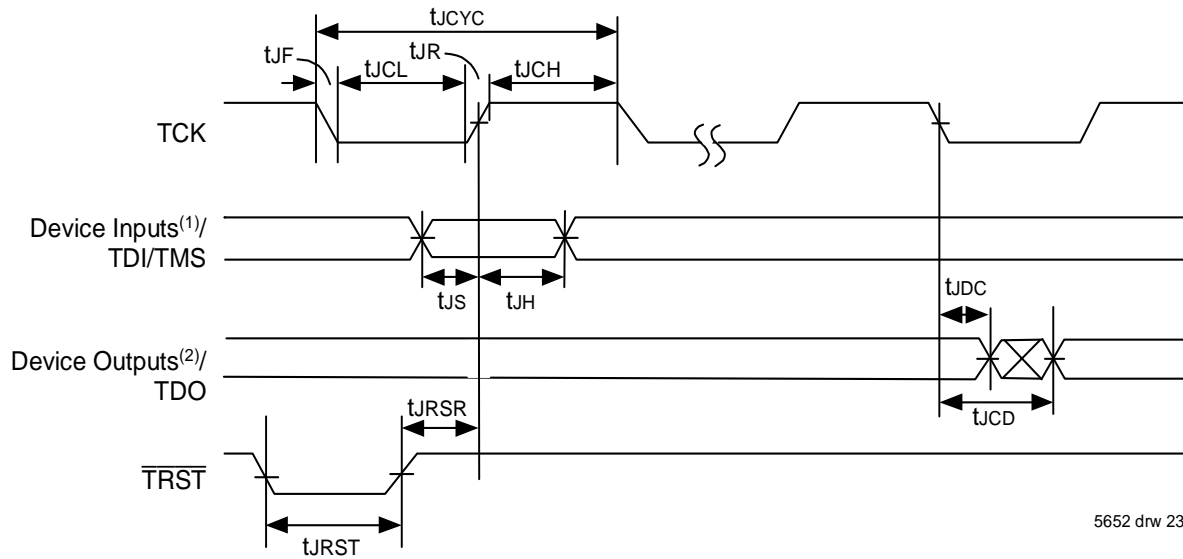
The IDT70T3339/19/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.



NOTE:

1. A19 is for IDT70T3339, A18 is for IDT70T3319, A17 is for IDT70T3399.

JTAG Timing Specifications



5652 drw 23

NOTES:

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics ^(1,2,3,4)

Symbol	Parameter	70T3339/19/99		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t_{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5652 tbl 15

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x333 ⁽¹⁾	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5652 tbl 16

NOTE:

1. Device ID for IDT70T3319 is 0x334. Device ID for IDT70T3399 is 0x335.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5652 tbl 17

System Interface Parameters

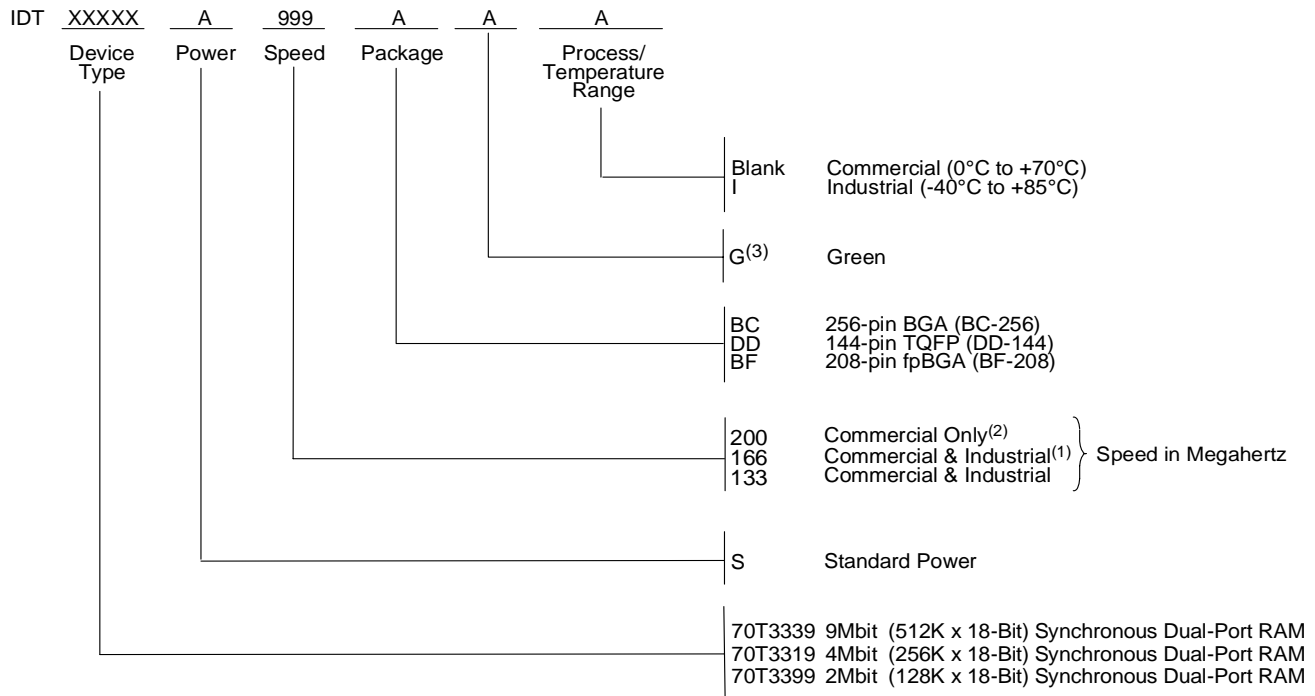
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except \overline{COLx} & \overline{INTx} outputs.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	0101, 0111, 1000, 1001, 1010, 1011, 1100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	0110, 1110, 1101	For internal use only.

5652 tbl 18

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and \overline{TRST} .
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



5652 drw 25

NOTES:

- 166MHz I-Temp is not available in the BF-208 package.
- 200Mhz is not available in the BF-208 and DD-144 packages.
- Green parts available. For specific speeds, packages and powers contact your local sales office.

IDT Clock Solution for IDT70T3339/19/99 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70T3339/19/99	2.5	LVTTTL	8pF	40%	200	75ps	5T2010	5T9010 5T905, 5T9050 5T907, 5T9070

5652 tbl 19

Datasheet Document History:

01/20/03:	Initial Datasheet
04/25/03:	Page 11 Added Capacitance Derating drawing Page 12 Changed t_{INS} and t_{INR} specs in AC Electrical Characteristics table
11/11/03:	Page 10 Updated power numbers in DC Electrical Characteristics table Page 12 Added t_{OFS} symbol and parameter to AC Electrical Characteristics table Page 21 Updated Collision Timing waveform Page 22 Added Collision Detection Timing table and footnotes Page 26 Updated HIGHZ function in System Interface Parameters table Page 27 Added IDT Clock Solution table
04/08/04:	Page 22 & 23 Clarified Sleep Mode Text and Waveforms Page 1 & 28 Removed Preliminary status
02/07/06:	Page 6 Added another sentence to footnote 4 to recommend that boundary scan not be operated during sleep mode Page 1 Added green availability to features Page 7 Changed footnote 2 for Truth Table I from \overline{ADS} , \overline{CNTEN} , $\overline{REPEAT} = V_{IH}$ to \overline{ADS} , \overline{CNTEN} , $\overline{REPEAT} = X$ Page 27 Added green indicator to ordering information
07/28/08:	Page 10 Corrected a typo in the DC Chars table footnotes



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